

To request the full datasheet, please visit <a href="https://www.intersil.com/products/isl95812">www.intersil.com/products/isl95812</a>

# Multiphase PWM Regulator for VR12.5, VR12.6 and VR12.6+ CPUs

#### ISL95812

Fully compliant with Intel VR12.5, VR12.6 and VR12.6+™ specifications, the ISL95812 provides a complete solution for microprocessor core power supply. It provides a Voltage Regulator (VR) with two integrated and one external gate drivers. The VR can be configured as 3-, 2- or 1-phase, providing maximum flexibility. The VR uses the serial control bus (SVID) to communicate with the CPU and achieves lower cost and smaller board area.

Based on Intersil's Robust Ripple Regulator (R<sup>3</sup>) technology™, the PWM modulator compared to traditional modulators, has faster transient settling time, variable switching frequency during load transients and has improved light load efficiency with its ability to automatically change switching frequency.

The ISL95812 has several other key features. The output supports DCR current sensing with single NTC thermistor for DCR temperature compensation or accurate resistor current sensing. The output comes with remote voltage sense, programmable  $V_{\mbox{\footnotesize{BOOT}}}$  voltage, programmable  $I_{\mbox{\footnotesize{CCMAX}}}$ , programmable voltage transition slew rate, adjustable switching frequency, overcurrent protection and Power-Good output.

### **Features**

- · Serial data bus
- Output configurable 3-, 2- or 1-phase using two integrated gate drivers
- · Precision core voltage regulation
- 0.5% system accuracy over-temperature
- Enhanced load line accuracy
- · Supports multiple current sensing methods
  - Lossless inductor DCR current sensing
- Precision resistor current sensing
- · Differential remote voltage sensing
- Programmable V<sub>BOOT</sub> voltage at start-up
- Resistor programmable I<sub>CCMAX</sub> and voltage transition slew rate
- Adaptive body diode conduction time reduction

## **Applications**

- · Notebook computers
- · Desktop computers

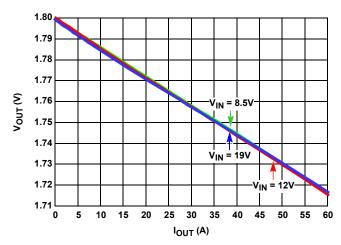


FIGURE 1. LOAD LINE REGULATION

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